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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/531,398	04/14/2005	Albert Jan Huitsing	NL02 1021 US	6508

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EXAMINER	
CRAWFORD, JASON	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 07/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/531,398	HUITSING, ALBERT JAN	
	Examiner	Art Unit	
	Jason Crawford	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1* is/are allowed.

6)☒ Claim(s) *2-11* is/are rejected.

7)☒ Claim(s) *1 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Abstract

Please submit an abstract on a separate sheet; it may simply be a copy of the abstract presented on the WIPO document.

Specification

Please add in the Continuation Data of the Application at the front of the Specification, this is required under 37 CFR 1.77(b) for Cross-Referencing to related Applications. For example, have a heading such as "**Continuation Data**" and below that heading something along the lines of "This Application is a 371 of PCT/IB03/04216 filed on 9/19/2003."

Claim Objections

1. Claims 1 and 11 are objected to because of the following informalities:

Claim 1 recites the limitation "the second inverter stage" in Line 4. There is insufficient antecedent basis for this limitation in the claim. Appropriate correction is required.

Claim 11 recites the limitation "A digital circuit unit comprising" however claim 2, which 11 is dependent on, recites of a "digital circuit unit." Claim 11 should take into account the antecedent basis established within claim 2 and recite, for example "The digital circuit unit further comprising an input terminal, the fail-safe circuit, a signal processing stage and an output terminal." Appropriate correction is required.

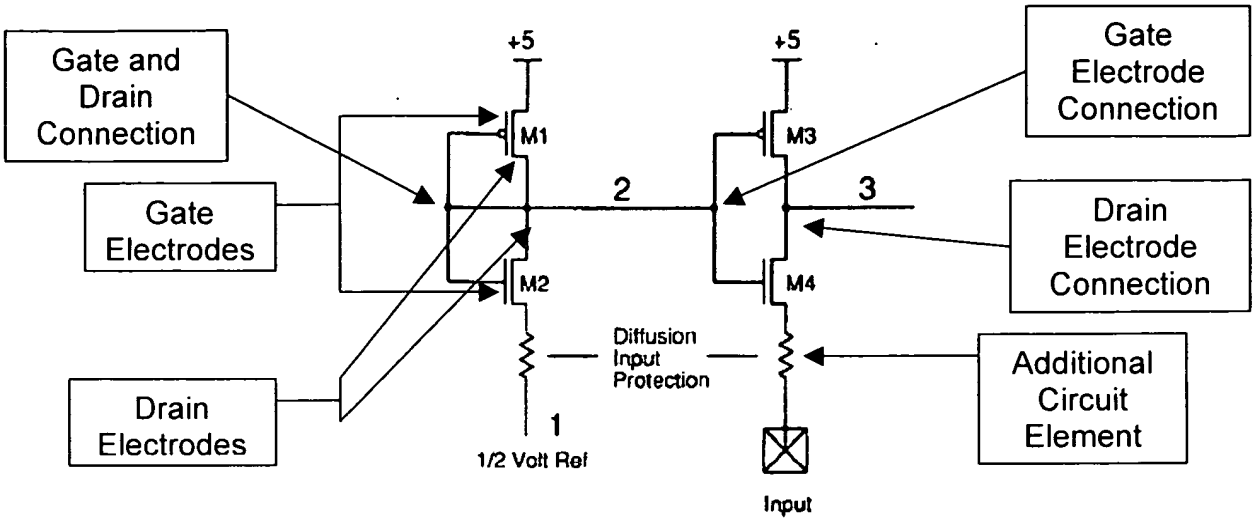
Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 2-7 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Knight (IEEE Journal of Solid State Circuits, vol. 23, no. 2, Pages 457-464, April 1988).

In regards to Claim 2, Knight discloses of a fail-safe circuit in Fig 11 for producing a fail-safe output signal (3) in case of an open circuit condition (i.e. if the input voltage is lower than the constant voltage of 2) of an input pad (Input) of a digital circuit unit comprising a first inverter stage (M1, M2) providing a constant switch level (at 2), a second inverter stage (M3, M4) providing a variable switch level that depends on the signal level of the input pad (Input) and comparing (at the source of M4 and gates of M3 and M4) the constant switch level (2) of the first inverter stage (M1, M2) with the variable switch level of the second stage (M3, M4) and providing an output signal at an output terminal (3) if the variable switch level of the second stage (M3, M4) is greater than the constant switch level (Fig 12 (c)) and an additional circuit element (Diffusion Input Protection resistor shown between M4 and Input), See **Reference Fig A** below) connected in series with the second inverter (M3, M4) for decreasing the switch level of the second inverter stage (M3, M4, the resistor will have a voltage drop across it, thereby decreasing the switch level). (Fig 11, Pages 461-463)



Reference Fig A (Claims 2-7)

In regards to Claim 3, Knight discloses of the first inverter stage (M1, M2) is a transistor stage (comprised of transistors M1, M2) and wherein the gate electrodes and the drain electrodes of the transistors (M1, M2) of the first inverter stage are connected to each other (See **Reference Fig A**). (Fig 11, Pages 461-463)

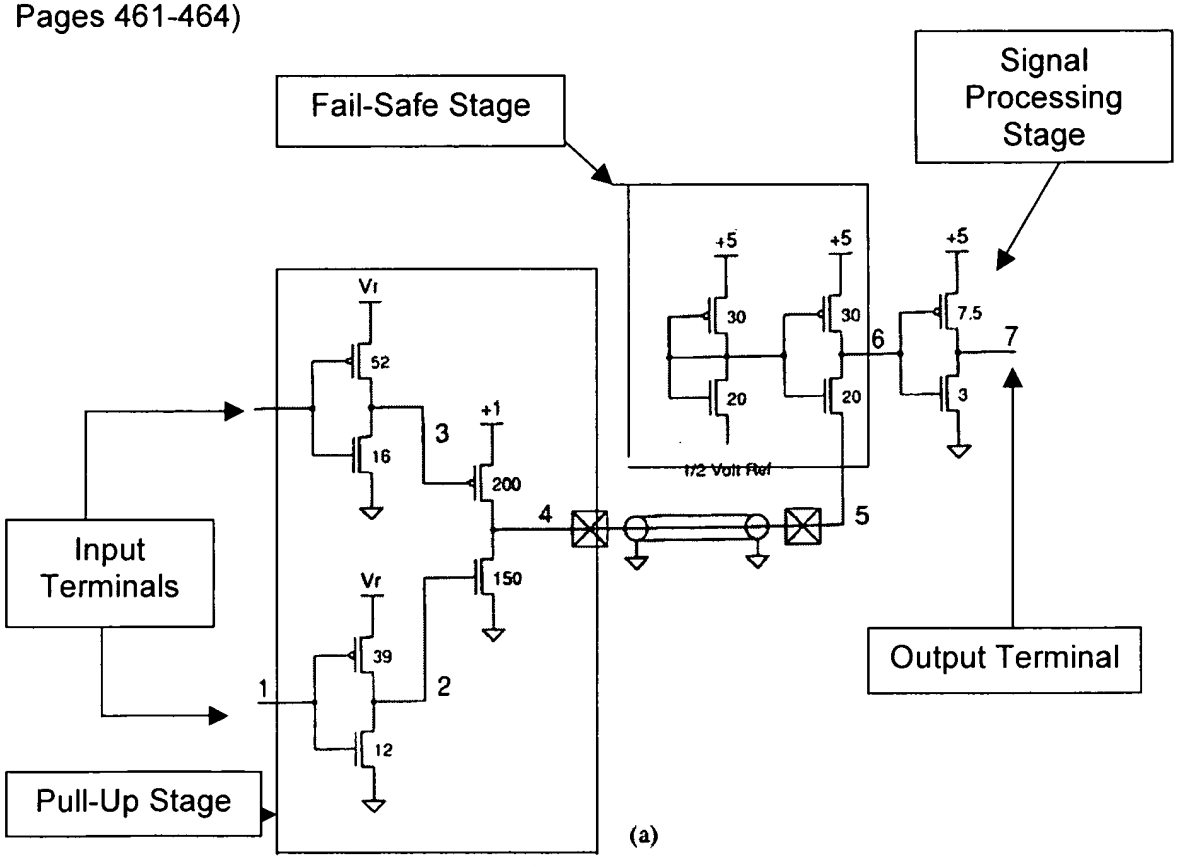
In regards to Claim 4, Knight discloses of the second inverter stage (M3, M4) is a transistor stage (comprised of transistors M3, M4) and wherein the gate electrodes of the transistors of the second inverter stage (M3, M4) are connected to each other (See **Reference Fig A**) and wherein the drain electrodes are connected to each other (**Reference Fig A**). (Fig 11, Pages 461-463)

In regards to Claim 5, Knight discloses of the gate electrodes of the second inverter stage (M3, M4) are connected (at 2) to the gate electrodes of the first inverter stage (M1, M2). (**Reference Fig A,** Fig 11, Pages 461-463)

In regards to Claim 6, Knight discloses of the input terminal (Input) is connected to a source electrode (source of M4) of the second inverter stage (M3, M4). (**Reference Fig A,** Fig 11, Pages 461-463)

In regards to Claim 7, Knight discloses of the output terminal (3) is connected to a drain electrode (drain of M3 and M4) of the second inverter stage (M3, M4). (**Reference Fig A,** Fig 11, Pages 461-463)

In regards to Claim 11, Knight discloses of the digital circuit of Fig 12(a) unit further comprising an input terminal, a pull-up stage, the fail-safe circuit, a signal processing stage and an output terminal (7). (See **Reference Fig B** below, Fig 12 (a), Pages 461-464)



Reference Fig B (Claim 11)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Knight (IEEE Journal of Solid State Circuits, vol. 23, no. 2, Pages 457-464, April 1988) in view of Graham (US 4918336).

In regards to the above claims, Knight discloses of a fail-safe circuit in Fig 11 as found within the explanation of claim 2 above wherein the additional circuit element is shown as a resistor. (Fig 11, Pages 461-463)

Knight does not directly disclose of the additional circuit for decreasing the switching level is a transistor in saturated mode gated by either VCC, as found in claim 9 or GROUND as found in claim 10.

Graham discloses of a semiconductor device comprising a resistor being the electrical equivalent to a transistor in saturated mode (i.e. a constant supply (either Vcc or Ground) is applied to its gate), specifically Graham shows that a PMOS in saturated mode has its gate tied to Ground and an NMOS in saturated mode has its gate tied to Vcc (Fig 14, Column 31-58).

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to replace the resistor of Knight with either an NMOS or PMOS transistor in saturated mode as taught by Graham because they are electrically

equivalent and discrete resistors are much larger than a transistor, therefore a saturated transistor would occupy less space on a semiconductor device.

Allowable Subject Matter

Claim 1 is allowed. The following is an examiner's statement of reasons for allowance:

In regards to Claim 1, the prior art of record does not directly disclose of of a method for producing a fail-safe output signal in case of an open circuit condition of an input pad of a digital circuit unit comprising providing a constant switch level in a first inverter stage, providing a variable switch level in a second inverter stage that depends on the signal level of the input pad, comparing the constant switch level of the first inverter stage with the variable switch level of the second stage, providing an output signal at an output terminal thereof if the switch level of the second stage is greater than the constant switch level and decreasing the switch level of the second inverter stage by an additional circuit element (connected in series with the second inverter *wherein a defined output being produced irrespective of the open circuit condition of an input pad* , nor would it have been obvious to one of ordinary skill in the art to do so.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Crawford whose telephone number is 571-272-6004. The examiner can normally be reached on Monday - Friday 7am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rex Barnie can be reached on 571-272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JMC

REXFORD BARNIE
SUPERVISORY PATENT EXAMINER